DI/AN CONTROLS INC.

BULLETIN 1-200

Universal Magnetic-Core Logic Elements

FEATURES

- **HIGHEST "LOGIC POWER"** — Unequalled per-element functional flexibility; each element provides up to *six* discrete input modes without supplemental circuitry of any kind.

- **MAXIMUM NOISE IMMUNITY** — Inherently low impedance level of element circuitry ensures high 1 : 0 ratios at minimum of pulse distortion. Circuitry inherently ...es pulse at every interrogation.

- **...NIMUM POWER-SUPPLY REQUIREMENTS** — Low-...ratio of average power to peak output power of any ...ailable digital element. Only one, unregulated, unipolar ...e required for all circuits . . . no clamps, taps, bias ...rns, or decoupling networks required.

- **...ION-VOLATILE STORAGE** — Logical state of the cir-cui... retained during power failure of any kind.

- **...L . . . LIGHT . . . TOUGH** — Highest *functional-*... of any macroelement. Optimum shape and proportions for high-density card mounting. Encapsulated for complete environmental protection, maximum shock and vibration resistance, and low internal thermal gradient.

- **HIGHEST OBTAINABLE CIRCUIT RELIABILITY** — Digital magnetic circuitry, which has been developed by DI/AN to a high degree of sophistication, is inherently extremely reliable. DI/AN magnetic elements have fewer components and fewer solder joints, and are completely encapsulated. In addition, over its many years of experience, DI/AN has developed production and testing techniques which ensure optimum product performance and reproducibility from lot to lot. A concentrated quality assurance program includes life testing, component evaluation and 100% production testing. Quality control standards conform to requirements of MIL-Q-9858. RESULT: more than 8 million module hours of operation without a failure.

- **PROVEN IN THOUSANDS OF APPLICATIONS** — Write for booklet entitled "Magnetic Logic in Space (A Report of Applications and Reliability)".

...RAL DESCRIPTION

...'s are *universal* logic elements with integral mag-...orage and delay capability. Appropriately interconnected, without additional circuitry of any kind, they can ...erform ...y logical function. A single DI/AN CTL (Core Tran... Logic element) will implement any of the following ...nctions: AND, OR, INHIBIT (AND NOT), BRANCH, ...DRIVE, BINARY COUNT and COMPLEMENT. ...L's are required to implement the EXCLUSIVE-... — and four CTL's form a full adder.

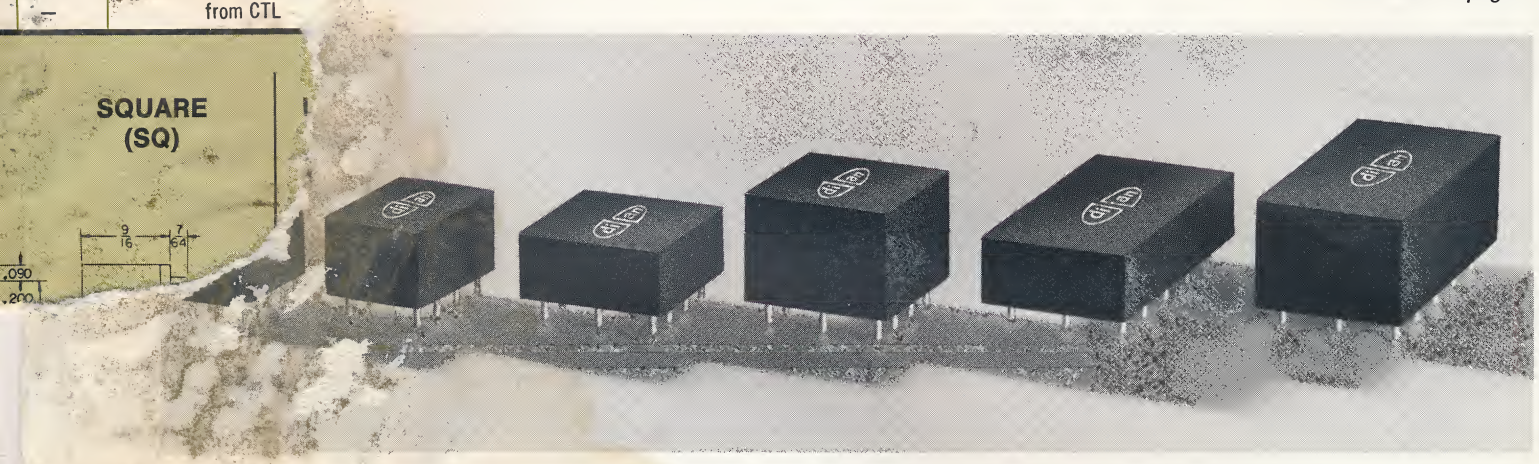
Because the C... utilizes only a small number of components ... being non-critical components with wide ...s), it provides a reliability unmatched by any ...ent. The ability of this single, basic element ...gic functions provides the ultimate in logic design simplicity, minimizing inventory problems and lowering costs at several stages of the design and production process.

The CTL offers the designer many other important advantages. Aging is negligible. Power supply requirements are minimal. Circuit packaging is convenient and inexpensive. Operating margins are wide, yet unit-to-unit performance control is very tight, which makes for easier, more straightforward designs that can be pushed to the limit. The CTL, in fact, is a very forgiving device, with broad tolerance for the poor waveforms, noise, etc., that plague the marginal circuit.

PRINCIPLES OF OPERATION

DI/AN Magnetic Core Logic Elements are simple in design and construction. They consist of a magnetic core containing

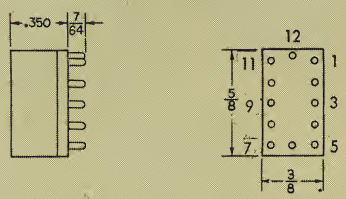
Continued on page 4



CHARACTERISTICS — MAGNETIC CO

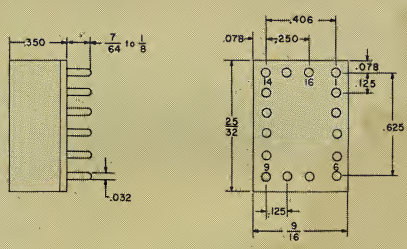
Model Designation	Packaging	Operating Freq. Range kilobits/sec	Maximum Operating Temp. (°C)	Power Supply Requirements (Nominal)			Inputs (Nominal)					
							Information					
							Current			Voltage		
				Voltage ±15%	Power (mW) All "ONE's"	Power (μW) Stand By	I_{in} (ma)	Voltage Drop Across Winding	Duration (μ sec)	E_{in} (volts)	Z_{in} (Ω)	Duration
LOGIC ELEMENTS												
CTL-100-P/N-12 CTL-100-P-3I-12 CTL-100-N-3I-12	SQ	0-100	55	12	140	60	20	1.2	5			
CTL-100-P/N-12S**	SQ	0-100	75	12	150	75	15	0.8	4			
CTL-250-P/N-12 CTL-250-P-3I-12 CTL-250-N-3I-12	SQ	0-250	55	12	250	60	30	1.0	2			
CTL-100-P/N-24 CTL-100-P-3I-24 CTL-100-N-3I-24	LSQ	0-100	125	24	280	30	18	1.5	5			
CTL-100-P/N-24	PB	0-100	125	$24^{+25\%}_{-10\%}$	150	25	12	0.5	4			
CTL-250-P/N-24	LSQ	0-250	125	24	400	30	30	0.8	2			
CTL-250-P-3I-28	PB	0-250	100	28	300	30	25	0.8	2			
CTL-250-P/N-28	PB	0-250	100	28	300	30	25	0.8	2			
CTL-250-P-4I-2S-28	MPB	0-250	100	28	300	30	25	0.8	2			
ACCESSORY ELEMENTS												
CTI-100-P-12	DSQ	0-100	55	12	400	60	—	—	—			
CTI-250-P-12	DSQ	0-250	55	12	500	100	—	—				
CTI-100-P/N-24	LDSQ	0-100	100	24	625	185	—	—				
CTI-250-P/N-24	LDSQ	0-250	100	24	750	200	—	—				
CTP-5-P-12	DSQ	0-5	55	12	840	84	—	—				
CTP-5-P-24	DSQ	0-5	100	24	1500	125	—	—	—	−5 to −20	250	1.0
TDL-100-24	LSQ	0-100	100	24	—	—	—	—	—	—	—	—

PICO-BIT® (PB)



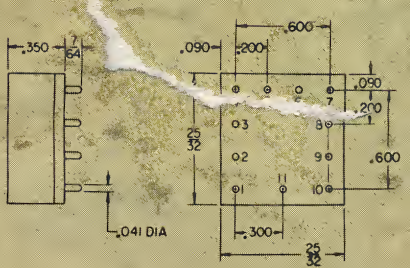
Note: Mating sockets available on order for breadboarding, etc.

MODIFIED PICO-BIT® (MPB)



Note: Mating sockets available on order for breadboarding, etc.

LOW SQUARE (LSQ)



Note: Mating sockets available on order for b

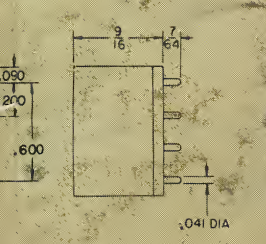
CORE LOGIC ELEMENTS & ACCESSORIES*

Trigger				Outputs (Nominal)							Logic Capability		
	Current			Voltage			Current				Fan Out		
							Undelayed		Delayed				
ration (μ sec)	I_{in} (ma)	IZ Drop Across Wdg. (volts)	Duration (μ sec)	Amplitude (volts)	1:0 Ratio	Permissible Z load (Ω/pf)	I peak (ma)	Duration (μ sec)	I peak (ma)	Duration (μ sec)	Trigger Using Delay Network	Trigger Not Using Delay Network	Information from Delay Network
		0.25	0.5	12	15:1	2000	100	0.5	30	4	—	—	—
		0.25	1.0	11	20:1	2000	100	1.0	20	4	—	—	—
		3.0	0.25	11.5	25:1	1500	100	0.25	30	0.85	—	—	—
			0.5	23	20:1	3000	100	0.5	30	3.0	—	—	—
			0.5	21	25:1	4000	100	0.5	30	1.5@ 20ma	—	—	—
			0.3	23	30:1	3000	100	0.3	30	1.4	—	—	—
			0.8	22	30:1	3000	150	0.5	30	1.4	—	—	—
			0.8	22	30:1	3000	150	0.5	30	2.0	—	—	—
			0.8	22	30:1	3000	150	0.5	30	2.0	—	—	—
nected,													
Tran- ing			—	−2.5	—	100	100	1.5	30	4	4	10	4
			—	−4	—	200	130	0.5	30	1.0	4	15	4
			—	+6	—	400	160	0.7	30	3.5	4	20	4
Bec			—	+6	—	400	125	0.45	30	1.5	4	20	4
			1.0	—	—	—	200	30 min	—	—	10 (A)	6 (B)	20 (C)
1.0	50 to 200	0.4	1.0	—	—	—	250	17 min	—	—	10 (A)	6 (B)	20 (C)
—	from CTL			—	—	—	100	0.5	—	—	—	20	—

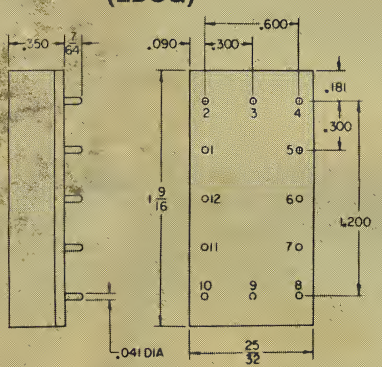
**Available on special order: high reliability device qualified to APOLLO Specs; T ≤ 105°C

††Beyond Threshold — (A) Via Input — (B) Reset via D.N. — (C) Via Shift

SQUARE (SQ)



LOW DOUBLE-SQUARE (LDSQ)



DOUBLE SQUARE (DSQ)

der for breadboarding, etc.

Note: Mating sockets available on order for breadboarding, etc.

Model Designation Code (use in ordering)

Output Polarity: P/N = Either Positive-Going or Negative-Going Output Pulse. P = Positive-Going Output Pulse. N = Negative-Going Output Pulse

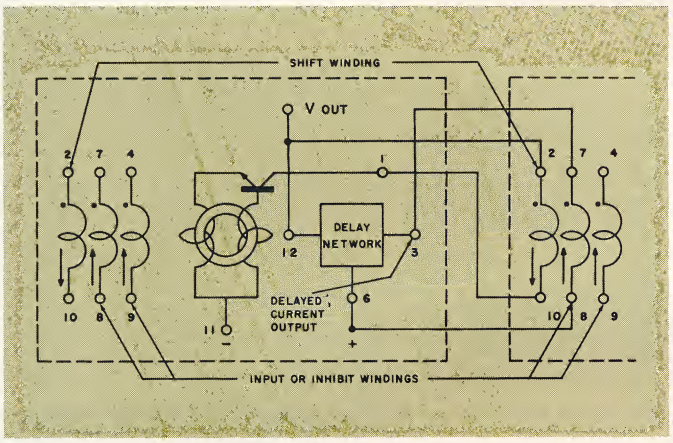
CTL–100–( )–( )–12 ( )–( )

- CTL: Denotes Element-Designation
- 100: Maximum Repetition Rate (Kilobits/Sec)
- ( ): Number of Logical Inputs (if more than two). Use only when Output Polarity specified is either "P" or "N"
- 12: Nominal Power-Supply Voltage
- ( ): Write an "S" here when specifying Silicon
- ( ): Module Package

***For additional information, please write for pertinent Module Specification Drawing.**

several windings, a transistor operated as a switch, and a simple passive delay network. Each CTL contains two or more information inputs, one or more shift inputs, and three types of outputs: (1) an undelayed voltage, which can be used to set static flip-flops, drive one-shots, etc.; (2) an undelayed current, ordinarily used to shift other CTL's; and, (3) a delayed current, commonly used to load or inhibit other CTL's.

Toroidal ferrite cores, having a rectangular hysteresis loop are employed in all DI/AN Magnetic Logic Elements. These cores have the ability to store information in the form of a stable residual magnetic field. An appropriate input pulse (applied to an *input winding*) will create a field that sets the core to the ONE condition. The application of a shift pulse to another winding (the *shift winding*) will, if of the correct polarity, reverse the magnetic field, resetting the core to ZERO. This flux reversal generates an output signal in the other windings on the core. Subsequent shift pulses of the established output polarity produce no significant output until the core is again set to the ONE state.

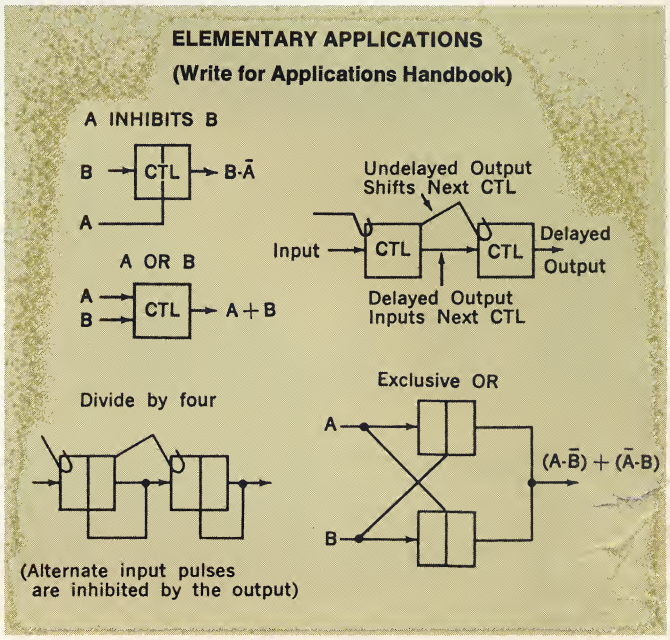


CTL shown wired for negative output to shift and load following CTL. Single CTL is enclosed by dotted line. Positive output achieved by simple change in external wiring. Pin numbers correspond to base diagram for the Pico-Bit®. Arrows show input direction.

The CTL module provides a connection arrangement that allows the transistor output to be directed through the shift windings of subsequent CTL's prior to being applied to its own delay network. This assures that the shift output precedes the load or inhibit output, thus preventing interaction between the shift and load (or inhibit) pulses. Connections are available on each CTL to provide either a positive or a negative output for a stored ONE.

SPECIAL ELEMENTS AND ACCESSORIES

CTI input amplifiers combine the functions of power amplification and signal-amplitude discrimination. Their input characteristics resemble a Schmitt trigger circuit. They are commonly used either to shift or to shift-and-load CTL's by amplifying low-energy signals that could not perform this function directly. A delay network is provided in the CTI for use in the shift-and-load operation. The CTI provides constant-amplitude, constant-width, output pulses es. ially independent of input-signal waveshape or repetition rate.



CTP elements operate as "pulse stretchers" and "pulse fortifiers", and are used to preset or reset one or more core circuits, through either their input or shift win CTP input can be either a voltage or a current p occur simultaneously nor at a rate in excess of 5 output is a current pulse of relatively long duratio

TDL pulse amplifiers are used to generate CTL shi when driven by the undelayed current output of anothe CTL. The use of this accessory circuit is recommended when it is logically necessary to shift more CTL's than can be dri by the unamplified, undelayed-current output pulse from one CTL.

CTRO elements are wide-pulse, high-peak-power pulse generators designed to furnish the current required to drive relay coils. Compatible with the CTL, they also have the logic capability of shift register elements. In a commo plication, CTRO's are connected in a shift register co guration in which a single ONE is stored. From this circuit, a predetermined sequence of relay closures can be obtained, as determined by the system logic. The output pulse width produced by a CTRO is controlled by an external timing capacitor, which can serve several CTRO's on a time-sharing basis.

These accessory modules are available in electrical and environmental ratings compatible with any of the standard DI/AN Magnetic-Core Logic Elements. Please feel free to consult the DI/AN Applications Engineering Department for specific circuit advice.

DI/AN CONTROLS, INC.

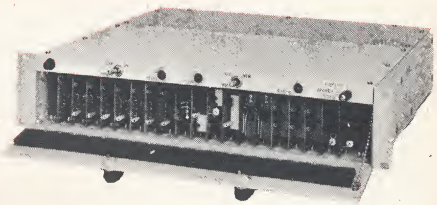
BULLETIN 61-40

magnetic digital/analog systems and components

SA SERIES BUFFERS

These buffers employ internally-addressed, coincident-current, magnetic core memories for data storage. They are designed for applications in which the data is to be read out of the memory in the same order in which it was originally written in. The internal address-selection circuitry, therefore, provides for sequential access to each of the memory locations in turn. Within this generic classification, however, a wide variety of data-manipulating programs may be chosen — there is a standard DI-AN design for almost every sequential-access buffer need, and a broad range of pre-engineered standard options which further extend the application scope of the SA series.

The outstanding features of the SA line are the exceptionally high **reliability** inherent in its all-solid-state, magnetic-storage/magnetic-control design, and the remarkably **compact construction** of even the highest-capacity, most flexible design. Both of these advantages are the result of exclusive DI-AN circuit innovations . . . particularly in the address generators and drivers. In these circuits (see page 3) the complex, high-dissipation static transistor/diode arrays used in conventional buffer equipment have been replaced by greatly-simplified **magnetic** shift-register and logic-element groups, drastically reducing the semi-conductor count, lowering the number and size of the power supplies required, and effecting significant economies in space and cost per bit manipulated. Most significantly, the dynamic magnetic circuitry provides greatly expanded operating margins — high ONE:ZERO ratios, minimum power supply and temperature tolerance, high stability.



Model SA-VB-INT-240/12 General-purpose buffer. Variable block-length independent load/unload programming. 2,880 bits of storage (240 characters of 12 bits each) in 3½" of rack height!

ULTRA-COMPACT
Up to 48,384 bits
in 10½" panel height!

ULTRA-RELIABLE
Simplified magnetic address, drive, and program circuitry cuts semiconductor count.

HIGH-CAPACITY
Available from 36 to 4,032 characters, up to 12 bits/character in standard sizes.

COMPLETE FLEXIBILITY
Hundreds of different standard sequence, capacity, program, and control combinations!

HIGH SPEED
Up to 200,000 characters/sec; access time, 2.5 μsec!

CLASS	DESCRIPTION	LOAD/UNLOAD SEQUENCE	TYPICAL APPLICATIONS AND OPERATING MODES
SA-VB-INT	General-purpose unit with maximum accommodation of external controls, and maximum provisions for DI-AN standard options, as described on pages 4 and 5.	Independent. May be interlaced in any arbitrary sequence.	Link between asynchronous equipments operating at different rates and processing different and variable blocks of information.
SA-1A-INT	Single-address unit. Provides for non-destructive readout (see options, page 5). Special versions available with fixed or selectable offset (or "skew") between load/unload addresses. This implements (among other possible operations) the "shifting" of information along the memory, one or more addresses per pass.	Interlaced unload-load of single addresses, processed sequentially.	Link between equipments operating under a single independent control. (e.g. sequential "scratch-pad" memory.) Provides for changing of selected data.
SA-1B-RESET	Single-block unit with destructive readout.	Load all of block, set to "Unload"; unload all of block, reset to "Load".	Link between equipments operating at different rates. (e.g. write in a block slowly, read it out at higher speed, processing an entire block at a time.)
SPECIAL-PURPOSE	See Page 6	See Page 6	See Page 6

GENERAL SPECIFICATIONS
(APPLY TO ALL SA SERIES BUFFERS)

STANDARD MEMORY CAPACITIES:

The SA series comprises fourteen standard designs, accomodating 36, 72, 144, 240, 336, 420, 540, 756, 1080, 1326, 1710, 2346, 3192, or 4032 characters of up to 12 bits/character. Hence, the largest standard memory accomodates 12 × 4032 = 48,384 bits. For larger capacities, see description of CUSTOM BUFFERS.

ADDRESSING:

In all SA series buffers, both loading and unloading proceed in a fixed sequence, from the first to the last address in the memory. The information stored in the memory is unloaded on a "first-in, first-out" basis. The "block length" — that is, the number of characters stored in one loading cycle — is variable and under external control. The circuitry for performing sequential address selection is entirely self-contained.

LOAD/UNLOAD FORMAT:

All the bits of a character are loaded or unloaded simultaneously, and are accepted and delivered in parallel. There are, therefore, as many signal input lines as there are bits/character. Since the output signals are in the form of complementary pairs, there are twice as many output lines as there are bits/character, two per bit. For serial formats, see CUSTOM BUFFERS.

LOAD/UNLOAD RATE:

(a) In the VB Buffers consecutive Load-Load or Unload-Unload Sync Pulses must be separated by 10 microseconds. Alternate Load-Unload Sync Pulses may be separated by only 5 microseconds.

(b) In the 1A Buffer, Unload and Load Sync Pulses must be separated by 5 microseconds or by 10 microseconds when only one Sync Pulse is furnished.

(c) In the SA-1B-RESET Buffer the Load and Unload Sync Pulses must be separated by 10 microseconds.

SYNCHRONIZATION:

In standard SA Series buffers, both the loading and the unloading processes are initiated by externally-generated pulses fed to the "LOAD SYNCH" and "UNLOAD SYNCH" terminals. As an option, a single "SYNCH" input can be provided, and a separate pair of "LOAD/UNLOAD" terminals is fed level signals which choose the desired mode, or the LOAD/UNLOAD cycle is predetermined and loading automatically follows the unloading process.

SYNCH SIGNALS:

In all standard SA designs, these signals must be negative-going pulses with duration between 1.0 and 2.0 microseconds, and rise times not exceeding 0.5 microseconds.

INPUT SIGNALS:

These buffers are designed to accept signals either as DC levels or as properly-synchronized pulses which establish the required levels at or before the rise of the load synch pulse, and maintain the required levels for at least 5.0 microseconds thereafter.

OUTPUT SIGNALS:

In standard designs, each bit of the character being unloaded appears as a complementary pair of DC levels on a pair of output terminals. The output levels are established 2.5 microseconds after the application of an unload synch pulse,* and persist until reset by the pulse.

* Standard access time is 2.5 μ sec. in all SA buffers.

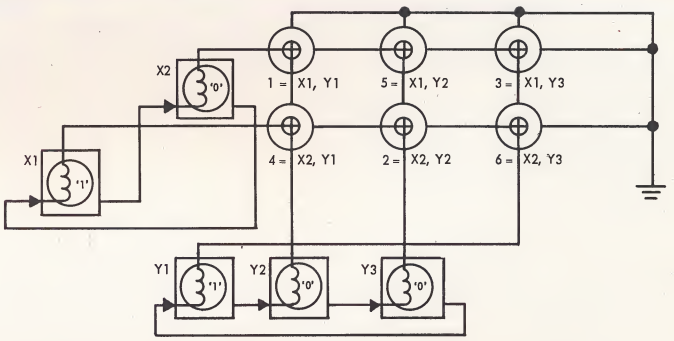
EXCLUSIVE DI/AN CIRCUITRY PROVIDES MAXIMUM RELIABILITY—OPTIMUM FLEXIBILITY

DYNAMIC MAGNETIC COUNTER – REGISTER – DRIVER

The cores in the coincident-current memory are driven by magnetic core-transistor shift registers which are also the address-generating counters. The use of a single dynamic magnetic element to perform all three functions (count to determine the next address position, store the count, and drive the memory cores) is the basic reason for the striking simplicity, high reliability, and compact construction of DI-AN buffers.

Magnetic core elements make ideal memory-core drivers. They are unaffected by large variations in load, power-supply voltage, ambient temperature, or input signal, and they require no standby power. They replace conventional circuits having many more transistors and diodes, and requiring far more complex and critical power supplies.

In the diagram, the address circuitry has been reduced, for simplicity, to a two-element "X" ring counter and a



three-element "Y" ring counter. A "one" is stored in each ring. As the counters are shifted, the read-out current passes through the input winding of the next stage of the ring before it enters an address line. Coincidence is achieved in the sequence indicated. Note that a single magnetic element serves for address positioning, address storage, and memory-core drive.

GENERAL-PURPOSE DESIGN PROVIDES COMPLETE LOAD/UNLOAD FLEXIBILITY, ARBITRARY BLOCK LENGTH

In the SA-VB-INT, the load and unload modes are independent because a full complement of address-generating/core-driving circuitry is provided for each function. In addition, block length may be arbitrarily determined (within the capacity limits of the memory) and may be different for load and unload.

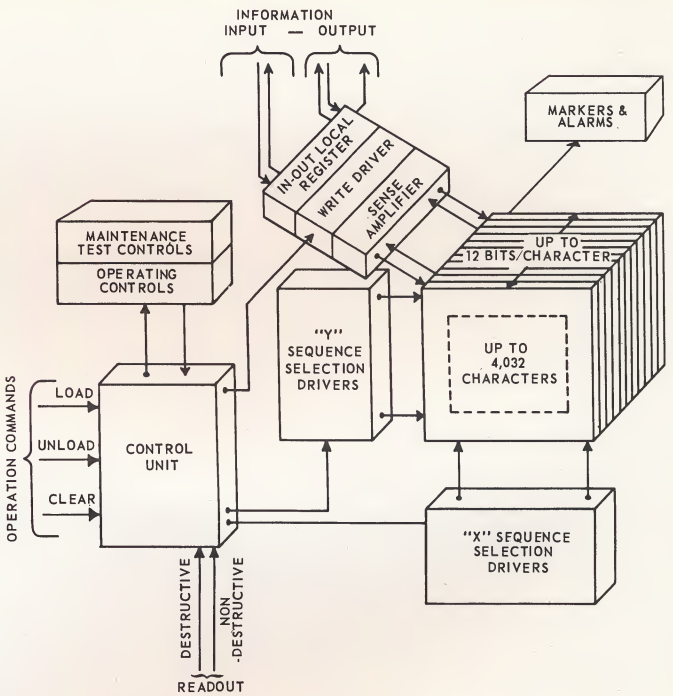
To permit full exploitation of the capabilities of this buffer, a number of input command facilities and condition signals are provided. These include:

Standard Features

- Marker Pulse to indicate that highest-order address has been loaded.
- Marker Pulse to indicate that highest-order address has been unloaded.
- Manual address reset.
- Manual memory clear.
- Internal Check program.

Standard Options

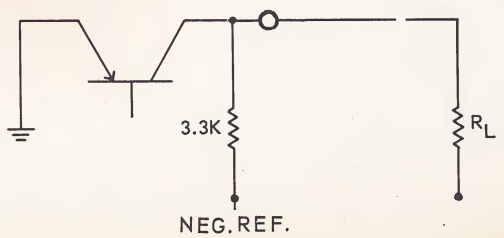
- Marker outputs at any pre-selected address.
- Electronic (plus manual) address reset.
- Electronic (plus manual) memory clear.
- Load-unload interlock.
- Pulse Information Inputs.
- Pulse Information Outputs.
- Fullness Control.



COMPLEMENTARY DC LEVEL OUTPUTS ARE 25MA VOLTAGE SOURCES WITH CHOICE OF REFERENCE POTENTIAL.

As an option, any external negative reference voltage up to –20 volts may be used. (This requires a slight wiring modification). When this is done, R_L must be of such value that total collector current does not exceed 25 ma.

STANDARD OUTPUT CONNECTIONS



STANDARD SIGNAL SPECIFICATIONS

SIGNAL	TYPE	"ONE" (OR "ON") VOLTS	"ZERO" (OR "OFF") VOLTS	IMPEDANCE	NOTES
LOAD SYNCH UNLOAD SYNCH	PULSE	–6 ±2	0	≥ 500 ohms (input) ≥ 220 ohms	duration, 1-2 μsec. Rise time 0.5 μsec. max.
INFORMATION INPUT	LEVEL	SA-VB-INT, SA-IA-INT: –0.2 to +5.0 SA-IB-Reset: –4.5 to –7.5	SA-VB-INT, SA-IA-INT: –4.5 to –7.5 SA-IB-Reset: –0.2 to +5.0	2.7K ohms (input)	may be properly-synchronized pulse – see page 2
INFORMATION OUTPUTS (complementary pair)	LEVEL	0.0 to –0.1	–5.5 to –6.5	See page 3	optionally, may be pulse.
MARKERS	PULSE	0	–6	load must exceed 1000 ohms	duration 1 μsec nominal. rise time, 0.5 μsec. max.
ADDRESS RESET	PULSE	–6 V	0	500 ohms (input)	duration 1 μsec nominal rise time, 0.5 μsec. max.
LOAD/UNLOAD SELECT	PULSE or LEVEL	–6 V	0	270 μμfd to Gnd. (input)	duration 1 μsec nominal. rise time, 0.5 μsec. max.
MEMORY CLEAR	PULSE	–6 V	0	1000 ohms (input)	duration 1 μsec. nominal. rise time, 0.5 μsec. max.
FULLNESS INDICATION	LEVEL	0	–6 V	load must exceed 1200 ohms	duration – level for duration of full condition

BUFFER FEATURES

S – Standard O – Optional NA – Not Applicable

FEATURE	CLASS		
	VB-INT	1B-R	1A-INT
Manual Address Reset	S	S	S
Manual Memory Clear	S	S	S
Double Synch (L & UL) Inputs	S	S	S
D.C. Level Info Inputs	S	S	S
D.C. Level Info Outputs	S	S	S
Internal Check Program	S	S	S
Marker Pulse Last Address Unload	S	S	S
Marker Pulse Last Address Load	S	S	S
Destructive Read-out	S	S	S
Electronic Address Reset (In addition to Manual)	O	S	O
Electronic Memory Clear (In addition to Manual)	O	S	O
Load-Unload Synch Discrimination	O	N.A.	O
Fullness Indication	O	O	N.A.
Emptiness Indication	O	O	N.A.
Remaining Available Storage Indication	O	O	N.A.
Parity Check – (internal error indication)	O	O	O
Parity Bit Generation (for external error check)	O	O	O
Extra markers-at pre-selected addresses	O	O	O
Pulse Info Outputs	O	O	O
Pulse Info Inputs	O	O	O
Single Sync Input with Separate Load-Unload Mode Selection	O	O	O
Field Selection	O	O	O
Non Destructive Readout	O*	N.A.	O

* with logical restrictions

MECHANICAL SPECIFICATIONS

SA Series buffers are manufactured in three standard 19" rack-mounting packages. The smallest has a panel height of only 3½", and a depth behind panel of 14". All SA Series buffers with capacities up to 240 12-bit characters fit in the 3½" high package. (When fewer bits per character are required, more than 240 characters may be accomodated in the 3½" configuration.)

For capacities above 240 12-bit characters two larger standard packages are employed. Up to 1326 12-bit characters may be accomodated in the 7" high unit, and up to 4,032 12-bit characters may be accomodated in the 10½" unit. Both of the larger units have depths of 14" behind the panel.

The power supplies used with the 3½ and 7 inch units can be furnished either integral with the buffer housing or for separate rack mounting. Most storage capacities of the 10½ inch housing permit an integral power supply.

See page 6 for other mechanical designs.

POWER INPUT

All SA Series buffers operate satisfactorily with power line input of 117 ±10% volts A.C., 60 ±2 cps. Power consumption ranges from 30 to 200 watts, depending on memory capacity. See page 6 for other line inputs.

ENVIRONMENT

All SA Series buffers are designed to give long, trouble-free service in environments ranging from 0° to 55° C, and 0 - 95% RH, at altitudes from 0 - 10,000 ft. See page 6 for special environments.

HOW TO SPECIFY
THE SA SERIES BUFFER YOU REQUIRE

1. Construct the model number of the required buffer as shown below:

SA	— VB – INT	— 4032 / 12	— PCG/EC/ER	— MOD
Denotes Sequential Access (SA) Series Buffers	This code indicates the program and logic class of the buffer, as selected from the chart on page 1.	Denotes maximum character capacity of memory	Denotes number of bits/character	These codes indicate options selected from list below. Omit if not required. Any number of options may be listed as shown.	Modification required. (See step 2, below)

2. Check the general specifications on page 2 and the detailed electrical and mechanical specifications on page 4. If one or more of these is incompatible with your needs, add the code "MOD" to the model number, and describe the required change in detail in your specification. DI-AN engineering will assign a special "MOD number" and advise costs.

STANDARD OPTIONS

These optional features are generally available on any SA Series buffer with which they are logically compatible, without significant delay or engineering charge, since they are all pre-engineered, using proven circuits and components.

PCA – PARITY CHECK AND ALARM

Continuously monitors parity of characters unloaded, and generates a DC level signal on a separate alarm line if parity is not achieved. This signal appears within 2.5 microseconds after the appearance of the output signal.

PBG – PARITY BIT GENERATION

Continuously monitors characters unloaded, and generates a parity bit on a pair of complementary output lines. Negligible delay in parity generation. Parity bit has same output level and source impedance as information bits.

EC – ELECTRONIC CLEAR

Provides input terminal which, when pulsed, clears memory within 150 microseconds. See page 4 for pulse specifications.

ER – ELECTRONIC ADDRESS RESET

Provides input terminal which, when pulsed, resets address register to first address. See page 4 for pulse specifications. Reset time is 25 microseconds.

AM (1, 2, . . .etc) – ADDRESS MARKERS

Provides two marker pulses (on two lines) one when a preselected address is loaded, and one when it is unloaded. Any number of markers may be ordered, up to the character capacity of the memory.

FI – FULLNESS INDICATOR

Provides DC level signals on a pair of output terminals which are set when and only when the memory is full. May be arranged to indicate when memory is nearly full. (This is a modification.) The signal appears within 2.5 microseconds after the last open address has been loaded. See page 4 for signal specifications.

PO – PULSE INFORMATION OUTPUT

Information outputs may be in the form of pulses rather than as dc levels. These pulses are positive-going from –6V to ground with a duration of 1.0 microseconds and a rise time of 0.5 microseconds or less when loaded with 1000 ohms returned to –6 V.

LUI – LOAD-UNLOAD INTERLOCK

Provides discrimination and required delay between load and unload synch pulses which arrive simultaneously or with less than minimum required time separation, so that information being written into or read out of the buffer is not destroyed.

NDR – NON-DESTRUCTIVE READOUT

Provides the capability of restoring in the buffer, at the next available address (as determined by logic) the information presented at the buffer outputs. (Model SA-1B-Reset excepted).

SPECIAL PURPOSE AND CUSTOM BUFFERS

As the leading manufacturer of special-purpose magnetic-digital equipment, DI-AN has designed a wide variety of buffers and data-manipulators. The list below can only indicate the range of our experience and capability. You are invited to bring your specific requirements to the attention of our engineering staff. You are assured of prompt, detailed, and expert assistance.

We are often able to modify one of the hundreds of buffer and control designs in our files to solve a new problem in a few hours, thus eliminating a costly and prolonged custom design effort.

RBP SERIES BUFFERS.

Provide storage and control to link computers, tapes, cards, etc., to rotary-bar printers, such as Anelex, Shephard, Potter. Ask for Bulletin 61-44, describing complete printing systems designed around the RBP series of buffers.

CTP SERIES BUFFERS.

Provide storage and control to implement corner-turning to side-fed card punches from end-fed card readers, tapes, computers, etc. This class of buffers can accomplish almost any one of the many "format conversion" assignments presented by the need to link equipments having dissimilar formats.

RA SERIES BUFFERS.

Provide random access to any address in the memory. Access time as low as 2.5 microseconds for a 4,096 character memory. Designs are available (R/SA Types) which combine random-search and sequential-access capability.

SC SERIES BUFFERS.

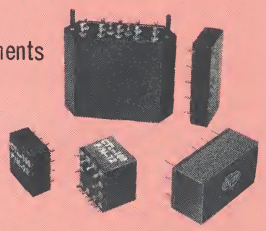
Provide storage and control to implement continuous sorting of serial-fed data into category selection devices. Format conversion includes required delay to satisfy the time and space displacement of the individual categories.

CUSTOM DESIGNS. Can be made to accomodate any of the following:

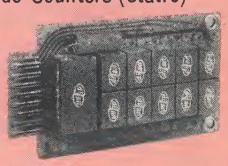
- High-Stress Environments. . .from the ground to outer space.
- Special Size and Weight Restrictions. . .satellites, missiles, aircraft.
- Higher Character Rates.
- Higher Character Capacities, more bits/character.
- Special Power Inputs — 400 cps, DC, poorly-regulated power lines.
- Field Selection requirements.

THE DI/AN PRODUCT LINE INCLUDES. . . .

BASIC SOLID-STATE CIRCUIT ELEMENTS
- Magnetic Register Elements
- Magnetic Logic Elements
- Static Flip-flop and Gate Elements



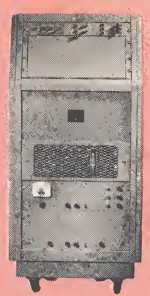
FUNCTIONAL PLUG-IN ASSEMBLIES OF BASIC ELEMENTS
- Shift-Register Assemblies (magnetic)
- Preset Digital Divider Assemblies (magnetic)
- Reversible Indicating Decade Counters (static)



LOGIC ELEMENT ASSEMBLY STRUCTURES
- Universal Logic Cards
- Magnetic Logic Breadboard
- Magnetic Logic Pack
- SRA Housing Structures

STORAGE SYSTEMS (Sequential-Access Magnetic BUFFERS)
- General Purpose Coincident-Current Magnetic-Storage Buffers
- Buffers for Controlling and Driving Rotary-Bar Printers
- Buffers for Data Format Conversion
- Buffers for Use in Digital Sorting Systems
- Buffers for Digital Count Totalizing

LOGICAL SYSTEMS
- Digital Time-Code Generators
- Digital Tape-Search Units
- Digital Programmers and Timers
- Special-Purpose Computer and Data Converters



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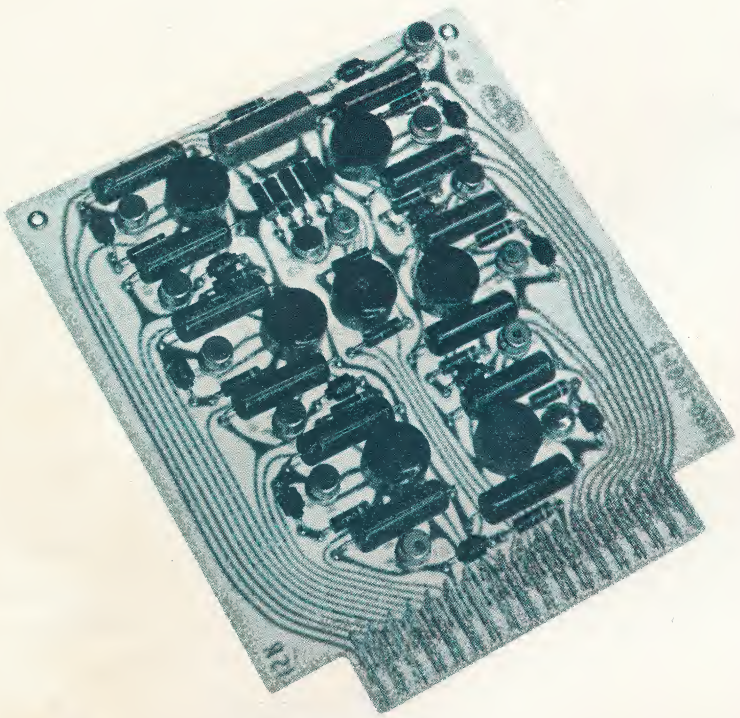

MAGNETIC INDUSTRIAL SHIFT REGISTER ASSEMBLY

MODEL ISR-12-100-P-12

FUNCTIONS

The circuits of the ISR card are one-core-per-bit, (single phase) elements with a transistor for each element to normalize the pulse and permit flexible connection over wide temperature and voltage margins. The card is used for counting, sorting and digital storage and delay in industrial materials handling, machine control and bookkeeping systems. It is especially valuable where high reliability and low cost are important factors. In conjunction with DI/AN CTLA Logic Assemblies, it provides a complete logic system capability requiring only two stock cards. The inputs and outputs of each of the 12 stages are available at the connector to permit parallel-to-serial or serial-to-parallel format conversion. By simple interconnections, the registers may be cascaded directly, without limit, for increased capacity. No additional components are needed to make a functional equipment.

DESCRIPTION

THE INDUSTRIAL SHIFT REGISTER CARD MODEL ISR-12-100-P-12 consists of 12 magnetic shift register stages with compatible driver mounted on a single plug-in card. Except for the potted cores, open circuit construction is used throughout to minimize cost. Components are mounted on an epoxy fiberglass etched circuit card with 35 phosphor-bronze, silver-plated and gold flashed ELCO connector pins. Individual mating connectors and standard housings capable of holding 21 or 42 cards are available. Connectors will be mounted in the housings by DI/AN at a nominal charge. Back boards and rear apron connectors will be wired to order.

FEATURES

- Magnetic Reliability and Noise Immunity
- Low Cost in Price and Design Time
- Data Not Lost with Power Shut Down
- Low Component Count
- Tolerant of Supply Variations
- Thoroughly Proven DI/AN Register Circuits
- Voltage or Current Outputs
- Flexibility — Separate input and outputs for each Stage

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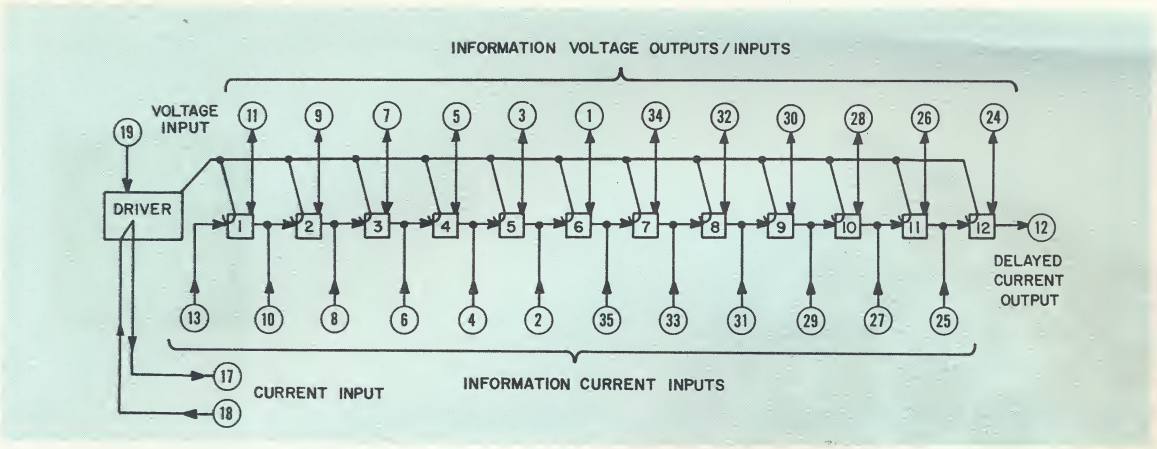


BLOCK DIAGRAM — INDUSTRIAL SHIFT REGISTER

OPERATION OF ISR CIRCUITS

The ISR circuit is electrically identical to that of the well-known DI/AN CTR-100 module. An operating cycle has three parts: Shift, Delay, Input. A shift pulse is applied simultaneously to all cores in a register. Those cores magnetized in the ONE state are switched by the shift pulse to the ZERO state. Switching from ONE to ZERO supplies drive current to a PNP transistor amplifier (See Schematic) which, in turn, loads the delay network. After the switching cycle is complete, the energy in the delay network appears at the output as a current pulse of the correct polarity to set the following core to the ONE state. Those cores initially magnetized in the ZERO state are **not** switched by the shift and no output appears. A following stage will thus be set to ONE if, and only if, the previous stage was in the ONE state before the shift pulse occurred. The entire pattern of ONE's and ZERO's is therefore moved one stage by each shift pulse. The first stage may be set to ONE by an appropriate input at any time between shift pulses. The Driver, which supplies shift current to the register stages, is similar to a register circuit except that it is returned to the ONE state after **each** shift pulse by a bias winding. It also incorporates a more complicated two-stage amplifier that permits a voltage input, as well as a current input, to trigger the driver. The diagram shows the logical interconnection and all pin connections for the twelve shift register stages and driver.

RELIABILITY

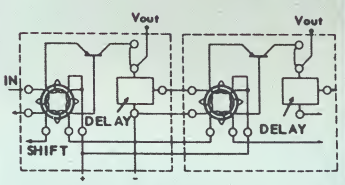
The long proven Reliability of the 100 KC shift register circuit arises from three principal facts.

1. Non-critical use of the transistor permits considerable Beta drift and a tremendous increase in leakage before the performance of the circuit is affected.
2. The circuit is intrinsically resistant to noise from relays, circuit breakers, etc., because of its very low impedance and limited operating speed.
3. Momentary power losses do not affect the state of the system. This can be of great significance in machine control or in the sorting of expensive products.

ACCESSORIES

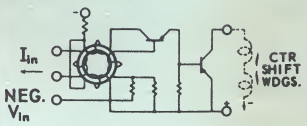
- Mating Connector — Model EV-35
- Housing — Model UL-12-1H (21 cards)

CTR



Schematic Diagram of a Magnetic Shift Register Employing Exclusive DI/AN High-Performance Core-Transistor Circuit (CTR). Dashed lines enclose contents of one Stage.

CTD



The CTD Shaper-Driver furnishes the necessary power gain and pulse standardization to provide a suitable current pulse for shifting compatible model CTR Shift Register Stages.

SPECIFICATIONS

Dimensions: 5 5/32 x 6 inches
Mounted on 0.8 inch centers

Shift Rate: 0 to 100 KC

Power Requirements: 12 V DC ± 15%

Register Input: A Current Pulse of 15 ma for approximately 5 μsec or not less than 6 ma for 10 μsec or more.

Register Outputs: A Current Pulse of 25 ma peak, approximately 4 μsec at ½ amplitude.

and

A Positive-Going Voltage Pulse of amplitude equal to supply voltage having 1 to 2 μsec rise time and approximately 4 μsec decay. A load of 1.5 K and 500 picofarads may be applied.

Driver Inputs: Current Input: 100 ma pulse of approximately 1.5 μsec duration.

or

Voltage Input: 10 volt, 0.5 to 1.0 μsec negative-going pulse from positive supply into 1000 ohms.

OPERATIONAL LIMITS

- -20° C to +40° C at rated frequency
- Humidity over temperature range is 100% without condensation
- Current on any one winding limited to 100 ma average current

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